IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

COMPLEX MEMORY, LLC, Plaintiff -against- TEXAS INSTRUMENTS, INC. and SVTRONICS, INC., Defendants	Civil Action No.: 2:17-cv-699 **JURY TRIAL DEMANDED**

DEFENDANT TEXAS INSTRUMENTS INCORPORATED'S ANSWER AND COUNTERCLAIMS TO PLAINTIFF COMPLEX MEMORY, LLC'S COMPLAINT

Defendant Texas Instruments Incorporated ("Defendant" or "TI") submits its answer to Plaintiff Complex Memory, LLC's ("Plaintiff" or "Complex Memory") Complaint.

TI's reproduction below of the headings and paragraphs set forth in the Complaint is solely for the purpose of convenience and is not, and should not be construed as, an admission by TI that any allegation or other statements in the headings or the paragraphs of the Complaint, whether explicit or implied, are true, correct, or admitted by TI. All allegations in Complex Memory's Complaint, including those in the headings, that TI does not expressly admit or deny in this Answer are specifically denied by TI.

PARTIES

1. Plaintiff Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 7116 Nicki Court, Dallas, Texas 75252.

TI's Response: TI is without knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 1 of the Complaint and therefore denies them.

2. On information and belief, Defendant TI is a Delaware corporation with a principal place of business at 12500 TI Boulevard, Dallas, TX 75243, and a manufacturing location at 6412 US-75, Sherman, TX 75090.

TI's Response: TI admits that it is a Delaware corporation with a principal place of business at 12500 TI Boulevard, Dallas, TX 75243, and a manufacturing location at 6412 US-75, Sherman, TX 75090.

3. On information and belief, Defendant SVTronics is a Texas corporation with a principal place of business at 3465 Technology Drive, Plano, TX 75074.

TI's Response: TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 3 of the Complaint and therefore, denies them.

JURISDICTION AND VENUE

4. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, *et seq.*, for infringement by TI and SVTronics of claims of U.S. Patent Nos. 5,890,195; 5,963,481; 6,658,576; 6,968,469; and 7,330,330 ("the Patents-in-Suit").

TI's Response: TI admits that Complex Memory purports to bring this action for patent infringement of U.S. Patent Nos. 5,890,195; 5,963,481; 6,658,576; 6,968,469; 7,730,330 ("the Patents-in-Suit"). TI denies that Complex Memory purports bring this action for patent infringement of U.S. Patent No. 7,330,330. Complaint (Dkt. No. 1) ¶ 19. TI denies that it is liable for patent infringement and that Complex Memory is entitled to any relief.

5. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

TI's response: TI states that the question of subject matter jurisdiction is a conclusion of law, rather than a statement of fact, to which no response is required. To the extent a response is required, TI admits that this Court has subject matter jurisdiction over patent disputes arising under the patent laws of the United States.

6. TI is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, (i) TI is headquartered in the State of Texas, (ii) TI maintains several office and manufacturing locations in the State of Texas; (iii) TI is registered to transact business in the State of Texas; and (iv) TI has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services in Texas.

TI's response: TI admits that it is subject to personal jurisdiction of this Court. TI admits that it is headquartered in the State of Texas and maintains several office and manufacturing locations in the State of Texas. TI also admits that it is registered to transact business in the State of Texas. However, TI denies it has committed or continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, or selling accused products and services in Texas.

7. Venue is proper as to TI in this district because, *inter alia*, on information and belief, TI maintains a regular and established place of business in this judicial district, and TI has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district.

TI's response: TI admits that venue is proper in the Eastern District of Texas, but TI denies it has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district.

8. SVTronics is subject to personal jurisdiction of this Court because, *inter alia*, on information and belief, (i) SVTronics is headquartered in the State of Texas, (ii) SVTronics maintains several office and manufacturing locations in the State of Texas; (iii) SVTronics is registered to transact business in the State of Texas; and (iv) SVTronics has committed and continues to commit acts of patent infringement in the State of Texas, including by making, using, offering to sell, and/or selling accused products and services in Texas.

TI's Response: The allegations of paragraph 8 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 8 of the Complaint and therefore, denies them.

9. Venue is proper as to SVTronics in this district because, *inter alia*, on information and belief, SVTronics is headquartered in, and maintains a regular and established place of business, in this judicial district, and SVTronics has committed and continues to commit acts of patent infringement in this judicial district, including by making, using, offering to sell, and/or selling accused products and services in this district.

TI's Response: The allegations of paragraph 9 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 9 of the Complaint and therefore, denies them.

SINGLE ACTION

10. This suit is commenced against TI and SVTronics pursuant to 35 U.S.C. § 299 in a single action because, *inter alia*, on information and belief, (i) the Defendants incorporate TI OMAP processors into the accused products; and (ii) Defendant SVTronics integrates and sells products based on processor designs by Defendant TI. Accordingly, the claims of this Complaint arise out of the same transaction, occurrence, or series of transactions or occurrences relating to the making, using, importing into the United States, offering for sale, or selling of the same accused product or process, and questions of fact common to all Defendants will arise in the action pursuant to 35 U.S.C. § 299.

TI's Response: TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 10 of the Complaint and therefore, denies them. TI states that the question of the same transaction, occurrence, or series of transactions or occurrences is a conclusion of law, rather than a statement of fact, to which no response is required. TI denies any and all remaining allegations in paragraph 10.

BACKGROUND

11. On March 30, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,890,195 ("the '195 Patent"), entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM".

TI's Response: TI admits that the face of U.S. Patent No. 5,890,195 ("the '195 Patent") bears an issue date of March 30, 1999, and is entitled "DRAM With Integral SRAM Comprising A Plurality Of Sets Of Address Latches Each Associated With One Of A Plurality Of SRAM." TI denies any

and all remaining allegations in paragraph 11.

12. G.R. Mohan Rao invented the technology claimed in the ’195 Patent.

TI’s Response: TI admits that the face of the ’195 Patent lists G.R. Mohan Rao as the inventor. TI denies any and all remaining allegations in paragraph 12.

13. On October 5, 1999, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 5,963,481 (“the ’481 Patent”), entitled “Embedded Enhanced DRAM, And Associated Method.”

TI’s Response: TI admits that the face of U.S. Patent No. 5,963,481 (“the ’481 Patent”) bears an issue date of October 5, 1999, and is entitled “Embedded Enhanced DRAM, And Associated Method.” TI denies any and all remaining allegations in paragraph 13.

14. Michael Alwais and Michael Peters invented the technology claimed in the ’481 Patent.

TI’s Response: TI admits that the face of the ’481 Patent lists Michael Alwais and Michael Peters as the inventors. TI denies any and all remaining allegations in paragraph 14.

15. On December 2, 2003, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,658,576 (“the ’576 Patent”), entitled “Energy-Conserving Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-Alive Processor With Keep-Alive Operating Instruction.”

TI’s Response: TI admits that the face of U.S. Patent No. 6,658,576 (“the ’576 Patent”) bears an issue date of December 2, 2003, and is entitled “Energy-Conserving Communication Apparatus Selectively Switching Between A Main Processor With Main Operating Instructions And Keep-

Alive Processor With Keep-Alive Operating Instruction." TI denies any and all remaining allegations in paragraph 15.

16. Howard Hong-Dough Lee invented the technology claimed in the '576 Patent.

TI's Response: TI admits that the face of the '576 Patent lists Howard Hong-Dough Lee as the inventor. TI denies any and all remaining allegations in paragraph 16.

17. On November 22, 2005, the United States Patent and Trademark Office duly and lawfully issued U.S . Patent No. 6,968,469 ("the '469 Patent"), entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored."

TI's Response: TI admits that the face of U.S. Patent No. 6,968,469 ("the '469 Patent") bears an issue date of November 22, 2005, and is entitled "System and Method For Preserving Internal Processor Context When The Processor Is Powered Down And Restoring The Internal Processor Context When Processor Is Restored." TI denies any and all remaining allegations of paragraph 17 of the Complaint.

18. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '469 Patent.

TI's Response: TI admits that the face of the '469 patent lists Marc Fleischmann and H. Peter Anvin as the inventors. TI denies any and all remaining allegations in paragraph 18.

19. On June 1, 2010, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,730,330 ("the '330 Patent"), entitled "System and Method For Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set."

TI's Response: TI admits that the face of U.S. Patent No. 7,730,330 ("the '330 Patent") bears an issue date of June 1, 2010, and is entitled "System and Method for Saving And Restoring A Processor State Without Executing Any Instructions From A First Instruction Set." TI denies any and all remaining allegations of paragraph 19 of the Complaint.

20. Marc Fleischmann and H. Peter Anvin invented the technology claimed in the '330 Patent.

TI's Response: TI admits that the face of the '330 Patent lists Marc Fleischmann and H. Peter Anvin as the inventors. TI denies any and all remaining allegations in paragraph 20.

21. Complex Memory is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

TI's Response: TI is without knowledge or information sufficient to form a belief as to the truth of the allegations of paragraph 21 and therefore, denies them.

COUNT I: INFRINGEMENT OF THE '195 PATENT BY TI

22. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 21 as if fully set forth herein.

23. Upon information and belief, TI has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the products identified in Attachment A ("Accused TI

Products").

TI's Response: TI denies the allegations contained in paragraph 23 of the Complaint.

24. For example, on information and belief, TI has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. For example, the Accused TI Products include Texas Instruments Inc.'s (TI's) AM437x platform. On information and belief, the TI AM437x platform includes an ARM Cortex-A9 Core, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, AM437x Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. In performing the method of claim 6, a processing core received an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller) or an address channel of a bus. The Accused TI Products compared the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." *Id.,* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller. When a match between the received address and a matching address stored in a one of the latches occurred, the Accused TI Products performed the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." *Id.* When a match between the received address and an address stored in one of the latches did not occur, the Accused TI Products performed the substeps of exchanging data between a location in the memory array addressed by the

received address and a selected one of the registers. "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." Ex. 4, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. When the match did not occur, the Accused TI Products further stored the received address in one of the latches corresponding to the selected register. For example, the Accused TI Products stored the received address, such as the tag, corresponding to the register being accessed, in the cache memory system registers, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers. *See* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. The Accused TI Products further modified the received address to generate a modified address. For example, the hardware in the Accused TI Products prefetches, for example, data stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 7.6.2 Data prefetching. *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher ("[P]refetch address = current address + (stride x programmed distance."). On information and belief, the Accused TI Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused TI Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." *See* Ex. 4 ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. The Accused TI Products then stored the modified address

in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag registers, such as the current TAG, set, index, and way registers.

TI's Response: TI admits that Ex. 3 states, "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." TI admits that Ex. 3 states, "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." TI admits that Ex. 4 states, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." TI denies any and all remaining allegations contained in paragraph 24 of the Complaint.

25. Upon information and belief, TI has committed the foregoing infringing activities without a license.

TI's Response: TI denies allegations contained in paragraph 25 of the Complaint.

COUNT II: INFRINGEMENT OF THE '576 PATENT BY TI

26. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 25 as if fully set forth herein.

27. Upon information and belief, TI has infringed, and continues to infringe, the ’576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

TI’s Response: TI denies allegations contained in paragraph 27 of the Complaint.

28. For example, on information and belief, TI has infringed at least claim 25 of the ’576 Patent by performing steps of an energy-conserving operating system. For example, the Accused TI Products include TI’s AM437x platform. On information and belief, the TI AM437x platform, includes an ARM Cortex-A9 Core, and performs the steps of claim 25 of the ’576 Patent. *See, e.g.*, Ex. 1, AM437x Datasheet. “Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power.” Ex. 7, ARM Cortex-A Series Version: 4.0 Programmer’s Guide, Chapter 20 Power Management. The Accused TI Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, the Accused TI Products activate a set of interrupt-handling instructions for the generic interrupt controller in connection with handling an interrupt in a standby mode, caused by, among others, the issuance of the WFI (wait for interrupt) instruction executed by a core. Ex. 8, ARM Generic Interrupt Controller Architecture version 2.0, Architecture Specification, § 3.7 Pseudocode details of interrupt handling and prioritization. If detecting a power-up signal, the Accused TI Products power up to provide a main operation that

utilizes main microprocessor circuitry and a set of main operating instructions. For example, when the main microprocessor circuitry, such as a core, is in the WFI low power state, an interrupt is detected by the generic interrupt controller, followed by powering up, such as enabling various clocks, to provide the main operation that utilizes that core and a set of main operating instructions, such as the instructions of the executed code following the WFI instruction. "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." Ex. 9, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20.4 Power Management Assembly language power instructions. The Accused TI Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, in the regular operating state, a WFI instruction detected by a core is a power-down signal. "Entry into WFI Standby mode is performed by executing the Wait For Interrupt instruction." Ex. 10 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 2.4.2 Cortex-A9 processor power control. If the WFI command is detected, the operating system places the system in the low-power WFI mode. "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." *Id.* In the Accused TI Products, said keep-alive operating instructions provide said energy- conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

TI's Response: TI admits that Ex. 7 states, "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." TI admits that Ex. 9 states, "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." TI admits that Ex. 10 states, "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." TI denies any and all remaining allegations contained in paragraph 28 of the Complaint.

29. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: TI denies allegations contained in paragraph 29 of the Complaint.

COUNT III: INFRINGEMENT OF THE '481 PATENT BY TI

30. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 29 as if fully set forth herein.

31. On information and belief, TI has infringed, and continues to infringe the ’481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating DDRxL and/or LPDDRx memories, including the Accused TI Products identified in Attachment A.

TI’s Response: TI denies allegations contained in paragraph 31 of the Complaint.

32. For example, on information and belief, TI infringes at least claim 16 of the ’481 Patent by performing a method of accessing data. On information and belief, the Accused TI Products, such as the AM572x Industrial Development Kit, include DDRxL memory, such as DDR3L. *See* Ex. 11, AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware User’s Guide (“The part number for the DDR3L SDRAM memory used is MT41K256M16HA- 125…”). DDR3L memory included in the Accused TI Products is a memory system comprising multiple banks with multiple rows. “4Gb: x4, x8, x16 DDR3L SDRAM Description,” Ex. 12 at p. 13-14 (“Row addressing is denoted as A[*n*:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.”). The Accused TI Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id.* at p. 12 (“The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.”). In TI’s DDR3L memory, the memory locations of the first memory row are disposed upon a substrate. *See* Ex. 11 (“The package used is the 96-ball TFBGA package.”). The Accused TI Products access the data stored at the memory locations identified in the first access request. Ex. 12. While the data stored at the memory locations identified by the first access request

is being accessed, the Accused TI Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See id.* at 12 ("As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time."). In the Accused TI Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. *See, e.g.*, Exs. 11-12. The Accused TI Products also access the data stored at the memory locations identified in the second access request. *Id.*

TI's Response: TI admits that Ex. 11 states, "The part number for the DDR3L SDRAM memory used is MT41K256M16HA-125." TI admits that Ex. 12 states, "Row addressing is denoted as A[n:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM." TI admits that Ex. 12 also states, "The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access." TI admits that Ex. 11 states, "The package used is the 96-ball TFBGA Package." TI admits that Ex. 12 states, "As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time." TI denies any and all remaining allegations contained in paragraph 32 of the Complaint.

33. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: TI denies the allegations contained in paragraph 33 of the Complaint.

COUNT IV: INFRINGEMENT OF THE '469 PATENT BY TI

34. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 33 as if fully set forth herein.

35. On information and belief, TI has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

TI's Response: TI denies the allegations contained in paragraph 35 of the Complaint.

36. For example, on information and belief, TI infringes at least claim 14 of the '469 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused TI Products, which are computer systems. The Accused TI Products include, for example, AM437x devices. On information and belief, AM437x devices include a processor, such as the microprocessor unit (MPU) subsystem. *See* Ex. 13 AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 3.1 Introduction at 151. The Accused TI Products include a first memory, such as one or more L1 caches, accessible by said processor (the MPU subsystem). *Id.* On information and belief, the Accused TI Products also include a second memory, on-chip memory RAM (OCM-RAM) accessible only to said processor. *Id.* OCM- RAM is internal to said processor, the MPU subsystem. *Id.* On information and belief, in the Accused TI Products, power

to said second memory is controlled separately from power to said processor and to said first memory, wherein power is maintained to said second memory (OCM- RAM) when power is removed from said processor (the MPU subsystem). For example, in the DeepSleep power mode, the MPU power domain, PD_MPU is OFF (except MPU OCM RAM retained). *See* Ex. 14, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.4.3 Power Modes at 256. On information and belief, in the Accused TI Products, the second memory is for maintaining internal context of said processor when power is removed from said processor. In the example of the DeepSleep power mode, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." *Id.*, § 6.4.3.3 DeepSleep at 257. On information and belief, the Accused TI Products also include a third memory external to said processor and accessible only to said processor. For example, the Accused TI Products include various L3 memories, some of which are external to the MPU subsystem but accessible only by the MPU subsystem. *See* Ex. 13, § 3.1 Introduction at 151; See, e.g., Ex. 15, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 2.1.1 at 140, fn. 1 ("The first 1MB of address space 0x0-0xFFFFF is inaccessible externally.") On further information and belief, certain memories containing bootcode and other sensitive and/or secure information, including High Security and/or Trustzone based memories, are also external to the MPU but accessible only by the MPU. On information and belief, in the Accused TI Products, the power to the third memory is controlled separately from power to said processor and to said first and second memories. For example, L3 memory belongs to the Peripheral power domain, PD_PER, which is separate from the MPU power domain, PD_MPU to which the MPU subsystem, the L1 cache, and the OCM-RAM belong. *See* Ex. 16, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.11 Device Modules and Power Management Attributes List at 298. In another example, the Accused TI

Products include a portion of L3 memory, the access to which is limited to high-security-enabled devices such as an A9 MPCore processor. On information and belief, in the Accused TI Products, the power to the third memory, L3 memory and the high- security access portions within it, is controlled separately from power to said processor and to said first and second memories. *Id.*

TI's Response: TI admits that Ex. 14 states, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." TI admits that Ex. 15 states, "The first 1MB of address space 0x0-0xFFFFF is inaccessible externally." TI denies any and all remaining allegations contained in paragraph 36 of the Complaint.

37. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: TI denies the allegations contained in paragraph 37 of the Complaint.

COUNT V: INFRINGEMENT OF THE '330 PATENT BY TI

38. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 37 as if fully set forth herein.

39. On information and belief, TI has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused TI Products identified in Attachment A.

TI's Response: TI denies the allegations contained in paragraph 39 of the Complaint.

40. For example, on information and belief, TI infringes at least claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused TI Products include a central processing unit, such as a TI OMAP 5 processor. *See* Ex. 17, OMAP 5432 EVM, Figure 1, OMAP5432 EVM Architectural Block Diagram. On information and belief, the OMAP 5432 CPU includes an ARM Cortex-A15 MPCore. *See* Ex. 18, OMAP5432 EVM, Chapter 2.3 OMAP5432 ES2.0 Processor. On information and belief, CPUs in the Accused TI Products execute the ARM 32-bit instruction set, Thumb 16-bit instruction set, and the Thumb 32-bit instruction set. *See* Ex. 19, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 4.2 The ARM instruction sets. On information and belief, the Accused TI Products include one or more registers holding a state, such as the CPSR, R13, and R14 registers. *See* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers. On information and belief, in the Accused TI Products, the CPU, is adapted, upon executing a first instruction from said first instruction set (such as an instruction from an application in an A32, T16, or T32 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save said state in a memory without executing any additional instructions from said first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs) (*see, e.g.*, Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")),

and (ii) to initiate an action that may cause the state of said registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which renders the above registers undefined). *See, e.g.*, Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers at p. 3-8 ("The reset values of R0-R14 are unpredictable"). On information and belief, in the Accused TI Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from said first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). *See, e.g.*, Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored."). In further addition, the OMAP CPU is similarly adapted when removing power from the NEON cores.

TI's Response: TI admits that Ex. 21 states, "Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory." TI admits that Ex. 20 states, "The reset values of R0-R14 are unpredictable." TI admits that Ex. 21 states, "To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored." TI denies any and all remaining allegations

contained in paragraph 40 of the Complaint.

41. On information and belief, TI has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: TI denies the allegations contained in paragraph 41 of the Complaint.

COUNT VI: INFRINGEMENT OF THE '195 PATENT BY SVTRONICS

42. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 41 as if fully set forth herein.

43. Upon information and belief, SVTronics has infringed the '195 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the products identified in Attachment B ("Accused SVTronics Products").

TI's Response: The allegations of paragraph 43 are not directed to TI, and therefore no

answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 43 of the Complaint and therefore, denies them.

44. For example, on information and belief, SVTronics has infringed at least claim 6 of the '195 Patent by performing a method of accessing blocks of data in a memory having a plurality of registers and a memory array. On information and belief, the Accused SVTronics Products include

Texas Instruments Inc.'s (TI's) AM437x platform. *See, e.g.*, Ex. 22, SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, the AM437x platform includes an ARM Cortex-A9 Core, including L1 and L2 cache memories having a plurality of registers and a memory array. *See, e.g.*, Ex. 1, AM437x Datasheet. *See also* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. In performing the method of claim 6, a processing core received an address through an address port such as an address input to a cache controller (*See* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller) or an address channel of a bus. The Accused SVTronics Products compared the received address with addresses previously stored in each of a plurality of latches, such as the latches holding addresses stored in cache memory. "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." *Id.,* Ex. 3, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.5 Cache controller. When a match between the received address and a matching address stored in a one of the latches occurred, the Accused SVTronics Products performed the substep of accessing a register corresponding to the latches storing the matching address through a data port. "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." *Id.* When a match between the received address and an address stored in one of the latches did not occur, the Accused SVTronics Products performed the substeps of exchanging data between a location in the memory array addressed by the received address and a selected one of the registers. "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." Ex. 4, ARM

Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. When the match did not occur, the Accused SVTronics Products further stored the received address in one of the latches corresponding to the selected register. For example, the Accused SVTronics Products stored the received address, such as the tag, corresponding to the register being accessed, in the cache memory system latches, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches. *See* Ex. 2, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8.4.1 Cache terminology. The Accused SVTronics Products further modified the received address to generate a modified address. For example, the hardware in the Accused SVTronics Products prefetches, for example, data stored at one or more prefetch addresses by modifying the address received by the processor for memory access. *See* Ex. 5 Cortex-A9 Revision: r4p1 Technical Reference Manual, Chapter 7.6.2 Data prefetching. *See also* Ex. 6 ARM Cortex-A15 MPCore Processor Technical Reference Manual, Chapter 7.4, L2 cache prefetcher ("[P]refetch address = current address + (stride x programmed distance."). On information and belief, the Accused SVTronics Products also modify the received address during a speculative lookup, including for speculative TAG lookup and speculative linefills. The Accused SVTronics Products further exchanged data between a location in the memory array addressed by the modified address and a second selected one of the registers. For example, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." *See* Ex. 4 ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 8 Caches. The Accused SVTronics Products then stored the modified address in of one of the latches corresponding to the second selected register. For example, during the hardware prefetch, in connection with the prefetched data being loaded into the cache, the

processor stored the modified address and/or tag in the latches storing addresses, including in the TAG RAM, address status and data bits, and in way, index, and tag register latches, such as the current TAG, set, index, and way register latches.

TI's Response: The allegations of paragraph 44 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI admits that Ex. 3 states, "When it receives a request from the core it must check to see whether the requested address is to be found in the cache. This is known as a cache look-up. It does this by comparing a subset of the address bits of the request with tag values associated with lines in the cache." TI admits that Ex. 3 states, "If there is a match (a hit) and the line is marked valid then the read or write will happen using the cache memory." TI admits that Ex. 4 states, "Whenever the core wants to read or write a particular address, it will first look for it in the cache. If it finds the address in the cache, it will use the data in the cache, rather than having to perform an access to main memory." TI is without knowledge or information sufficient to form a belief as to the truth of any and all remaining allegations contained in paragraph 44 of the Complaint and therefore, denies them.

45. Upon information and belief, SVTronics has committed the foregoing infringing activities without a license.

TI's Response: The allegations of paragraph 45 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 45 of the Complaint and therefore, denies them.

COUNT VII: INFRINGEMENT OF THE '576 PATENT BY SVTRONICS

46. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraph 1 through 45 as if fully set forth herein.

47. Upon information and belief, SVTronics has infringed, and continues to infringe, the '576 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

TI's Response: The allegations of paragraph 47 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 47 of the Complaint and therefore, denies them.

48. For example, on information and belief, SVTronics has infringed at least claim 25 of the '576 Patent by performing steps of an energy-conserving operating system. On information and belief, the Accused SVTronics Products include TI's AM437x platform. *See, e.g.*, Ex. 22, SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, the AM437x platform, includes an ARM Cortex-A9 Core, and performs the steps of claim 25 of the '576 Patent. *See, e.g.*, Ex. 1, AM437x Datasheet. "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." Ex. 7, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20 Power Management. The Accused

SVTronics Products activate a set of keep-alive operating instructions for providing an energy-conserving operation that utilizes keep-alive microprocessor circuitry. For example, the Accused SVTronics Products activate a set of interrupt-handling instructions for the generic interrupt controller in connection with handling an interrupt in a standby mode, caused by, among others, the issuance of the WFI (wait for interrupt) instruction executed by a core. Ex. 8, ARM Generic Interrupt Controller Architecture version 2.0, Architecture Specification, § 3.7 Pseudocode details of interrupt handling and prioritization. If detecting a power-up signal, the Accused SVTronics Products power up to provide a main operation that utilizes main microprocessor circuitry and a set of main operating instructions. For example, when the main microprocessor circuitry, such as a core, is in the WFI low power state, an interrupt is detected by the generic interrupt controller, followed by powering up, such as enabling various clocks, to provide the main operation that utilizes that core and a set of main operating instructions, such as the instructions of the executed code following the WFI instruction. "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." Ex. 9, ARM Cortex-A Series Version: 4.0 Programmer's Guide, Chapter 20.4 Power Management Assembly language power instructions. The Accused SVTronics Products power down to provide said energy-conserving operation in which said main microprocessor circuitry is deactivated, if detecting a power-down signal. For example, in the regular operating state, a WFI instruction detected by a core is a power-down signal. "Entry into WFI Standby mode is performed by executing the Wait For Interrupt instruction." Ex. 10 Cortex-

A9 Revision: r4p1 Technical Reference Manual, Chapter 2.4.2 Cortex-A9 processor power control. If the WFI command is detected, the operating system places the system in the low-power WFI mode. "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." *Id.* In the Accused SVTronics Products, said keep-alive operating instructions provide said energy-conserving operation requiring less computation power as compared with said main operating instructions. *Id.*

TI's Response: The allegations of paragraph 48 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI admits that Ex. 7 states, "Power management aware operating systems dynamically change the power states of cores, balancing the available compute capacity to the current workload, while attempting to use the minimum amount of power. Some of these techniques dynamically switch cores on and off, or place them into quiescent states, where they no longer perform computation. This means they consume very little power." TI admits that Ex. 9 states, "The WFI instruction has the effect of suspending execution until the core is woken up by one of the following conditions: • An IRQ interrupt, even if the CPSR I-bit is set. • An FIQ interrupt, even if the CPSR F-bit is set. • An asynchronous abort. • A Debug Entry request, even if JTAG Debug is disabled. In the event of the core being woken by an interrupt when the relevant CPSR interrupt flag is disabled, the core will implement the next instruction after WFI." TI admits that Ex. 10 states, "WFI and WFE Standby modes disable most of the clocks in a processor, while keeping its logic powered up. This reduces the power drawn to the static leakage current, leaving a tiny clock power overhead requirement to enable the device to wake up." TI is without knowledge or information sufficient to form a belief as to the truth of any and

all remaining allegations contained in paragraph 48 of the Complaint and therefore, denies them.

49. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: The allegations of paragraph 49 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 49 of the Complaint and therefore, denies them.

COUNT VIII: INFRINGEMENT OF THE '481 PATENT BY SVTRONICS

50. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraphs 1 through 50 as if fully set forth herein.

51. On information and belief, SVTronics has infringed, and continues to infringe the '481 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating DDRxL and/or LPDDRx memories, including the Accused SVTronics Products.

TI's Response: The allegations of paragraph 51 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 51 of the Complaint and therefore, denies them.

52. For example, on information and belief, SVTronics infringes at least claim 16 of the '481

Patent by performing a method of accessing data. On information and belief, the Accused SVTronics Products, such as the OMAP5432EVM With COM8Q Connector and the SOM437X board, include DDRxL memory, such as DDR3L. *See* Ex. 23 OMAP5432 EVM With COM8Q Connector Specification (retrieved from svtronics.com/5432C). *See also* Ex. 11, AM572x Industrial Development Kit (IDK) Evaluation Module (EVM) Hardware User's Guide ("The part number for the DDR3L SDRAM memory used is MT41K256M16HA-125…"). *See* also Ex. 24, SVTronics SOM437x System-On-Module datasaheet. DDR3L memory included in the Accused SVTronics Products is a memory system comprising multiple banks with multiple rows. "4Gb: x4, x8, x16 DDR3L SDRAM Description," Ex. 12 at p. 13-14 ("Row addressing is denoted as A[*n*:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM."). The Accused SVTronics Products generate a first access request for accessing data stored at memory locations of a first memory row. *Id.* at p. 12 ("The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access."). In SVTronics' DDR3L memory, the memory locations of the first memory row are disposed upon a substrate. *See* Ex. 11 ("The package used is the 96-ball TFBGA package."). The Accused SVTronics Products access the data stored at the memory locations identified in the first access request. Ex. 12. While the data stored at the memory locations identified by the first access request is being accessed, the Accused SVTronics Products generate a second access request for accessing data stored at memory locations of a second memory row. For example, in a burst read operation, while data from the previous access request is being accessed, the subsequent requests access data stored in different rows of another bank. *See id.* at 12 ("As with standard DDR SDRAM, the pipelined,

multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.”). In the Accused SVTronics Products, the memory locations of the second memory row are also disposed upon the substrate at which the memory locations of the first memory row are disposed. *See, e.g.*, Exs. 11-12. The Accused SVTronics Products also access the data stored at the memory locations identified in the second access request. *Id.*

TI's Response: The allegations of paragraph 52 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI admits that Ex. 11 states, “The part number for the DDR3L SDRAM memory used is MT41K256M16HA-125.” TI admits that Ex. 12 states, “Row addressing is denoted as A[n:0] . . . DDR3 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 8-bank DRAM.” TI admits that Ex. 12 also states, “The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.” TI admits that Ex. 11 states, “The package used is the 96-ball TFBGA Package.” TI admits that Ex. 12 states, “As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.” TI is without knowledge or information sufficient to form a belief as to the truth of any and all remaining allegations contained in paragraph 52 of the Complaint and therefore, denies them.

53. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: The allegations of paragraph 53 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 53 of the Complaint and therefore, denies them.

COUNT IX: INFRINGEMENT OF THE '469 PATENT BY SVTRONICS

54. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraphs 1 through 53 as if fully set forth herein.

55. On information and belief, SVTronics has infringed, and continues to infringe the '469 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

TI's Response: The allegations of paragraph 55 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 55 of the Complaint and therefore, denies them.

56. For example, on information and belief, SVTronics infringes at least claim 14 of the '469 by making, using, selling, or offering to sell in the United States, or importing into the United States the Accused SVTronics Products, which are computer systems. On information and belief, the Accused SVTronics Products include, for example, TI's AM437x platform. *See, e.g.*, Ex. 22,

SVTronics AM437x boards (retrieved from svtronics.com/am4). On information and belief, AM437x devices include a processor, such as the microprocessor unit (MPU) subsystem. *See* Ex. 13 AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 3.1 Introduction at 151. The Accused SVTronics Products include a first memory, such as one or more L1 caches, accessible by said processor (the MPU subsystem). *Id*. On information and belief, the Accused SVTronics Products also include a second memory, on-chip memory RAM (OCM-RAM) accessible only to said processor. *Id*. OCM-RAM is internal to said processor, the MPU subsystem. *Id*. On information and belief, in the Accused SVTronics Products, power to said second memory is controlled separately from power to said processor and to said first memory, wherein power is maintained to said second memory (OCM-RAM) when power is removed from said processor (the MPU subsystem). For example, in the DeepSleep power mode, the MPU power domain, PD_MPU is OFF (except MPU OCM RAM retained). *See* Ex. 14, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.4.3 Power Modes at 256. On information and belief, in the Accused SVTronics Products, the second memory is for maintaining internal context of said processor when power is removed from said processor. In the example of the DeepSleep power mode, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." *Id*., § 6.4.3.3 DeepSleep at 257. On information and belief, the Accused SVTronics Products also include a third memory external to said processor and accessible only to said processor. For example, the Accused SVTronics Products include various L3 memories, some of which are external to the MPU subsystem but accessible only by the MPU subsystem. *See* Ex. 13, § 3.1 Introduction at 151; See, e.g., Ex. 15, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 2.1.1 at 140, fn. 1 ("The first 1MB of address space 0x0-0xFFFFF is inaccessible externally.") On further information and belief, certain memories containing

bootcode and other sensitive and/or secure information, including High Security and/or Trustzone based memories, are also external to the MPU but accessible only by the MPU. On information and belief, in the Accused SVTronics Products, the power to the third memory is controlled separately from power to said processor and to said first and second memories. For example, L3 memory belongs to the Peripheral power domain, PD_PER, which is separate from the MPU power domain, PD_MPU to which the MPU subsystem, the L1 cache, and the OCM-RAM belong. *See* Ex. 16, AM437x ARM Cortex-A9 Processors Technical Reference Manual, § 6.11 Device Modules and Power Management Attributes List at 298. In another example, the Accused SVTronics Products include a portion of L3 memory, the access to which is limited to high-security-enabled devices such as an A9 MPCore processor. On information and belief, in the Accused SVTronics Products, the power to the third memory, L3 memory and the high-security access portions within it, is controlled separately from power to said processor and to said first and second memories. *Id.*

TI's Response: The allegations of paragraph 56 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI admits that Ex. 14 states, "In addition, power to OCMC RAM is maintained to preserve information internally during DeepSleep." TI admits that Ex. 15 states, "The first 1MB of address space 0x0-0xFFFFF is inaccessible externally." TI is without knowledge or information sufficient to form a belief as to the truth of any and all remaining allegations contained in paragraph 56 of the Complaint and therefore, denies them.

57. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: The allegations of paragraph 57 are not directed to TI, and therefore no answer is

required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 57 of the Complaint and therefore, denies them.

COUNT X: INFRINGEMENT OF THE '330 PATENT BY SVTRONICS

58. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

TI's Response: TI restates and incorporates by reference its answers to paragraphs 1 through 57 as if fully set forth herein.

59. On information and belief, SVTronics has infringed, and continues to infringe, the'330 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States or importing into the United States products incorporating ARM Cortex-A9 and/or ARM Cortex-A15 architectures, including the Accused SVTronics Products identified in Attachment B.

TI's Response: The allegations of paragraph 59 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 59 of the Complaint and therefore, denies them.

60. For example, on information and belief, SVTronics infringes at least claim 103 of the '330 Patent by making, using, selling, or offering to sell in the United States, or importing into the United States the above-identified devices which comprise a Central Processing Unit ("CPU") for executing instructions from a first instruction set. On information and belief, the Accused SVTronics Products, such as the OMAP5432EVM With COM8Q Connector or the Jorjin

OMAP4460 Application Processor Modules include a central processing unit, such as a TI OMAP 4 or OMAP 5 processor. *See, e.g.*, Ex. 23. *See also* Ex. 17, OMAP 5432 EVM, Figure 1, OMAP5432 EVM Architectural Block Diagram. On information and belief, the OMAP 5432 CPU includes an ARM Cortex-A15 MPCore. *See* Ex. 18, OMAP5432 EVM, Chapter 2.3 OMAP5432 ES2.0 Processor. On information and belief, the OMAP 4 processor includes an ARM Cortex-A9 MPCore. On information and belief, CPUs in the Accused SVTronics Products execute the ARM 32-bit instruction set, Thumb 16-bit instruction set, and the Thumb 32-bit instruction set. *See* Ex. 19, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 4.2 The ARM instruction sets. On information and belief, the Accused SVTronics Products include one or more registers holding a state, such as the CPSR, R13, and R14 registers. *See* Ex. 20, ARM Cortex-A Series Programmer's Guide Version 4.0, Chapter 3.1 Registers. On information and belief, in the Accused SVTronics Products, the CPU, is adapted, upon executing a first instruction from said first instruction set (such as an instruction from an application in an A32, T16, or T32 instruction set, which is different from the instruction set used for kernel and operating system tasks, before entering dormant mode) to (i) save said state in a memory without executing any additional instructions from said first instruction set (for example, by saving the state without executing any instructions from the instruction set to which the first instruction belongs) (*see, e.g.*, Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.")), and (ii) to initiate an action that may cause the state of said registers to become undefined (for example, exiting dormant mode requires applying a 'Reset' to the CPU cores, which renders the above registers undefined). *See, e.g.*, Ex. 20, ARM Cortex-A Series Programmer's Guide Version

4.0, Chapter 3.1 Registers at p. 3-8 ("The reset values of R0-R14 are unpredictable"). On information and belief, in the Accused SVTronics Products, the CPU is further adapted to, in response to an event to restore the saved state of said registers from said memory without executing any additional instructions from said first instruction set. For example, when exiting dormant mode, the CPU restores state to the above registers without executing instructions from the instruction set to which the first instruction belongs (for example, by executing instructions from one of the other two instruction sets; such that, if the first instruction set is A32, instructions from T32 or A64 are executed upon exiting the dormant mode). *See, e.g.*, Ex. 21, Cortex-A15, Revision: r2p1, Technical Reference Manual, Chapter 2.4.3. Power modes ("To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored."). In further addition, the OMAP CPU is similarly adapted when removing power from the NEON cores.

TI's Response: The allegations of paragraph 60 are not directed to TI, and therefore no answer is required. To the extent that a response is required, TI admits that Ex. 21 states, "Before entering Dormant mode, the architectural state of the Cortex-A15 processor, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory." TI admits that Ex. 20 states, "The reset values of R0-R14 are unpredictable." TI admits that Ex. 21 states, "To exit from Dormant mode to Run mode, the SoC must perform a full power-on reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the Cortex-A15 processor exits the power-on reset sequence, and the architectural state must be restored." TI is without knowledge or information sufficient to form a belief as to the truth of any and all remaining allegations contained in paragraph 60 of the Complaint and therefore, denies them.

61. On information and belief, SVTronics has committed and continues to commit the foregoing infringing activities without a license.

TI's Response: The allegations of paragraph 61 are not directed to TI, and therefore no

answer is required. To the extent that a response is required, TI is without knowledge or information sufficient to form a belief as to the truth of the allegations contained in paragraph 61 of the Complaint and therefore, denies them.

PRAYER FOR RELIEF

WHEREFORE, Complex Memory prays for the judgment in its favor against each of the Defendants, jointly, and severally, and specifically, for the following relief:

A. Entry of judgment in favor of Complex Memory against the Defendants on all counts;

B. Entry of judgment that the Defendants have infringed the Patent-in-Suit;

C. An order permanently enjoining the Defendants from infringing the Patent-in-Suit;

D. Award of compensatory damages adequate to compensate Complex Memory for the Defendants' infringement of the Patent-in-Suit, in no event less than a reasonable royalty as provided by 35 U.S.C. § 284;

E. Complex Memory's costs;

F. Pre-judgment and post-judgment interest on Complex Memory's award; and

G. All such other and further relief as the Court deems just or equitable.

TI's Response: No response to the Prayer for Relief is necessary. To the extent a response is required, TI denies that Plaintiff is entitled to any of the relief requested against TI.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. Proc., Plaintiff hereby demands trial by jury in this action of all claims so triable.

TI's Response: There are no allegations of fact contained in this paragraph and therefore, no response is required.

DEFENSES

TI asserts the following defenses to Complex Memory's claims without admitting or acknowledging that it bears the burden of proof as to any of the defenses asserted. TI reserves the right to amend its Answer to add additional defenses.

FIRST DEFENSE: NON-INFRINGEMENT

62. TI does not infringe and has never infringed any valid and enforceable claim of the Patents-In-Suit, as defined in Complex Memory's Complaint, whether literally or under the doctrine of equivalents, and as such, is without any liability to Complex Memory.

SECOND DEFENSE: INVALIDITY

63. The asserted claims of the Patents-In-Suit are invalid for failure to comply with the requirements of the patent laws of the United States, including provisions of 35 U.S.C. §§ 101, 102, 103, or 112.

THIRD DEFENSE: LIMITATION ON DAMAGES

64. Any recovery of damages by Complex Memory is limited in whole or in part by 35 U.S.C. §§ 252, 286, 287, 288, 307, or 318.

FOURTH DEFENSE: EQUITABLE DEFENSES

65. Complex Memory's claims for relief concerning the Patents-In-Suit are barred, in whole

or in part, under the principles of equity, including estoppel, prosecution history estoppel and/or disclaimer, and/or unclean hands.

FIFTH DEFENSE: LICENSE DEFENSE

66. Complex Memory's attempted enforcement of the Patents-In-Suit against TI is barred in whole or in part by one or more of (1) express or implied license, (2) release, (3) patent exhaustion, and (4) stand-still agreements.

SIXTH DEFENSE: LIMITATIONS FOR SALES COVERED BY 28 U.S.C. § 1498(a)

67. Complex Memory's remedies are limited under 28 U.S.C. § 1498(a) to the extent that Complex Memory accuses products or services that are provided, made, or used by or for the government of the United States of America.

SEVENTH DEFENSE: UNAVAILABILITY OF INJUNCTIVE RELIEF

68. Complex Memory is not entitled to injunctive relief or any other equitable relief at least because any alleged injury to Complex Memory is not irreparable and because, had Complex Memory been injured, it would have an adequate remedy at law. Moreover, at least one of the Patents-In-Suit is expired.

EIGHTH DEFENSE: EXTRATERRITORIALITY

69. Complex Memory's claim for patent infringement is precluded in whole or in part to the extent that any accused functionality or acts are located or performed outside of the United States.

COUNTERCLAIMS

Pursuant to Federal Rule of Civil Procedure 13, Texas Instruments Incorporated ("TI" or "Counterclaimant") alleges counterclaims against Complex Memory, LLC ("Complex Memory") as follows:

PARTIES

1. TI is a Delaware corporation with a principal place of business at 12500 TI Boulevard, Dallas, TX 75243.

2. Upon information and belief, and according to Complex Memory's Complaint, Complex Memory is a limited liability company organized and existing under the laws of the State of Texas, having its principal place of business at 7116 Nicki Court, Dallas, Texas 75252.

JURISDICTION AND VENUE

3. This is an action for declaratory judgment of non-infringement and invalidity of U.S. Patent Nos. 5,890,195 ("the '195 Patent"); 5,963,481 ("the '481 Patent"); 6,658,576 ("the '576 Patent"); 6,968,469 ("the '469 Patent"); and 7,730,330 ("the '330 Patent") (collectively, "the Patents-in-Suit"). This Court has subject matter jurisdiction over this claim pursuant to 28 U.S.C. §§ 1331, 1338(a), 2201, and 2202.

4. Venue is proper in the Eastern District of Texas, under 28 U.S.C. §§ 1391 and 1400, as a result of Complex Memory having filed this action in this District. By filing its Complaint in this District, Complex Memory has consented to personal jurisdiction and venue.

BACKGROUND

5. On October 13, 2017, Complex Memory filed suit against TI, claiming infringement of the Patents-in-Suit.

6. In its Complaint, Complex Memory alleges that it "is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement." Complaint (Dkt. No. 1) ¶ 21.

7. An actual, substantial, and justiciable controversy, within the meaning of 28 U.S.C.

§ 2201 and 2202, exists between Complex Memory and TI concerning the validity of the Patents-in-Suit. This controversy is of sufficient immediacy and reality to warrant the issuance of a declaratory judgment.

COUNT ONE

(DECLARATORY JUDGMENT OF PATENT INVALIDITY OF THE '195 PATENT)

8. TI incorporates paragraphs 1–7 of its Counterclaims as if fully set forth herein.

9. The claims of the '195 Patent are invalid for failure to comply with one or more requirements of patentability, including 35 U.S.C. §§ 101, 102, 103, and/or 112.

10. TI is entitled to a declaratory judgment that the claims of the '195 Patent are invalid.

COUNT TWO

(DECLARATORY JUDGMENT OF PATENT INVALIDITY OF THE '481 PATENT)

11. TI incorporates paragraphs 1–10 of its Counterclaims as if fully set forth herein.

12. The claims of the '481 Patent are invalid for failure to comply with one or more requirements of patentability, including 35 U.S.C. §§ 101, 102, 103, and/or 112.

13. TI is entitled to a declaratory judgment that the claims of the '481 Patent are invalid.

COUNT THREE

(DECLARATORY JUDGMENT OF PATENT INVALIDITY OF THE '576 PATENT)

14. TI incorporates paragraphs 1–13 of its Counterclaims as if fully set forth herein.

15. The claims of the '576 Patent are invalid for failure to comply with one or more requirements of patentability, including 35 U.S.C. §§ 101, 102, 103, and/or 112.

16. TI is entitled to a declaratory judgment that the claims of the '576 Patent are invalid.

COUNT FOUR

(DECLARATORY JUDGMENT OF PATENT INVALIDITY OF THE '469 PATENT)

17. TI incorporates paragraphs 1–16 of its Counterclaims as if fully set forth herein.

18. The claims of the ’469 Patent are invalid for failure to comply with one or more requirements of patentability, including 35 U.S.C. §§ 101, 102, 103, and/or 112.

19. TI is entitled to a declaratory judgment that the claims of the ’469 Patent are invalid.

COUNT FIVE

(DECLARATORY JUDGMENT OF PATENT INVALIDITY OF THE ’330 PATENT)

20. TI incorporates paragraphs 1–19 of its Counterclaims as if fully set forth herein.

21. The claims of the ’330 Patent are invalid for failure to comply with one or more requirements of patentability, including 35 U.S.C. §§ 101, 102, 103, and/or 112.

22. TI is entitled to a declaratory judgment that the claims of the ’330 Patent are invalid.

DEMAND FOR JURY TRIAL

TI demands a jury trial on all issues that may be so tried.

PRAYER FOR RELIEF

For THESE REASONS, TI respectfully requests that this Court enter judgment in its favor and grant the following relief:

A. Dismiss Plaintiff’s Complaint against TI with prejudice;

B. Deny all relief requested by Plaintiff in its Complaint;

C. Enter judgment that TI has not infringed (whether literally or by the doctrine of equivalents) any valid and enforceable asserted claim of the Patents-in-Suit, and does not infringe (whether literally or by the doctrine of equivalents) any valid and enforceable asserted claim of the Patents-in-Suit;

D. Enter judgment and/or declare that the claims of the Patents-in-Suit are invalid;

E. An order declaring that this is an exceptional case and awarding TI its costs,

expenses, and reasonable attorney fees under 35 U.S.C. § 285 and all other applicable statutes, rules, and common law;

F. Any such other relief as the Court may deem appropriate and just under the circumstances.

Dated: January 10, 2018

Respectfully submitted,

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ATTORNEY FOR TEXAS INSTRUMENTS INCORPORATED

CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3) this 10th day of January 2018. Any other counsel of record will be served by facsimile transmission and/or first-class mail.

Amanda A. Abraham

AMANDA A. ABRAHAM